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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,777	11/19/2001	Craig Nemecek	CYPR-CD01208M	2046

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EXAMINER	
JACOB, MARY C	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/989,777	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-9 and 16-24* is/are allowed.

6)☒ Claim(s) *1-3,10-12 and 25* is/are rejected.

7)☒ Claim(s) *4-6,13-15 and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/9/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Mary Jacob is now the Examiner assigned to this application. Correspondence information is given below.

2. The reply filed 12/11/07 has been received and considered. Claims 1-28 have been presented for examination.

Information Disclosure Statement

3. Reference "V" on the IDS filed 11/9/07 has not been considered since no copy of the reference was supplied.

Allowable Subject Matter

4. Claims 4-6, 13-15 and 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 7-9, 16-24 are allowed.

Claim Rejections - 35 USC § 112

6. The rejections of Claims 1-6, 10-15, 25-28 under 35 U.S.C. 112, first paragraph recited in the 9/11/07 Office Action have been withdrawn in view of Applicant's arguments (see page 12) and in view of further consideration by the Examiner.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. The prior art used for these rejections is as follows: U.S. Patent 7,236,921 to Nemecek et al. (Henceforth referred to as "**Nemecek et al.**").

9. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

10. Claims 1-3, 10-12 and 25, are rejected under 35 U.S.C. 102(e) as being anticipated by Nemecek et al.

11. In regards to Claim 1, Nemecek et al. teaches the following limitations:

> 1. A method for performing a sleep operation in a system that includes a device under test and an emulator device, said method comprising:
>
> a) executing instructions on said device under test;

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

> b) emulating the functions of said device under test by operating said emulator device in lock-step fashion with said device under test; and

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

> c) performing a sleep operation, comprising:

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

c1) upon receiving a first signal from an operating program that indicates that a sleep function is to be performed, initiating said sleep function at said device under test;

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

c2) in response to said initiating said sleep function, turning off one or more clock of said device under test; and

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

c3) discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock.

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

12. In regards to Claim 2, Nemecek et al. teaches the following limitations:

2. The method of Claim 1 wherein said clock comprises an internal CPU clock.

(See Nemecek et al., especially: col.17, lines 3-6)

13. In regards to Claim 3, Nemecek et al. teaches the following limitations:

3. The method of Claim 2 wherein said first signal is generated by said device under test and is transmitted internally to a register that indicates that a sleep function is to be performed.

(See Nemecek et al., especially: col.16, lines 41-44 and Item 716 in Figure 9.)

14. In regards to Claim 10, Nemecek et al. teaches the following limitations:

10. A method for performing a sleep operation, comprising:

executing a sequence of instructions by a device under test, said device under test including at least one clock for generating clock signals;

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

receiving a first signal from an operating program at a register of said device under test that indicates that a sleep function is to be initiated;

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

initiating said sleep function at said device under test upon receipt of said first signal;

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

turning off said at least one clock of said device under test; and

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

discontinuing execution of instructions that are performed in lock-step by

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

said emulator device upon said turning off of said clock.

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

15. In regards to Claim 11, Nemecek et al. teaches the following limitations:

11. The method according to claim 10 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

(See Nemecek et al., especially: col.13, line 54 to col.14, line 3, and Fig.6, Item 220)

16. In regards to Claim 12, Nemecek et al. teaches the following limitations:

12. The method of Claim 11 wherein said at least one clock includes a microcontroller CPU clock.

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

17. In regards to Claim 25, Nemecek et al. teaches the following limitations:

25. An in-circuit emulation system comprising;

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

a device under test that executes a sequence of instructions, said device under test operable, upon receiving a first signal from an operating program to initiate a sleep function at said device under test and to turn off a clock of said device under test responsive to said initiation; and

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

an emulator device for emulating the functions of said device under test, said emulator device operable so as to execute said sequence of instructions in lock-step fashion with said device under test, said emulator device operable, upon said turning off of said clock to discontinue execution of said sequence of instructions at said emulator device.

(See Nemecek et al., especially: col.16, line 21 to col.17, line 37)

Response to Arguments

18. Applicant's arguments filed 12/11/07 with respect to Claims 1, 10 and 25 have been fully considered but they are not persuasive.

19. Applicant argues that Nemecek fails to teach or suggest a sleep function (page 14, paragraph 1). However, Nemecek teaches or suggests a sleep function (column 16, lines 34-41).

20. Applicant argues that Nemecek fails to teach or suggest how or when the microcontroller goes into sleep mode, thereby failing to teach or suggest receiving a first signal from an operating program that indicates that a sleep operation is to be performed (page 13, last paragraph, page 14, first paragraph). Nemecek teaches or suggests a sleep function (column 16, lines 34-41). Further, the specification recites in the "Background of the Invention", "*...During the course of the analysis, the microcontroller can perform a sleep function in which the microcontroller "sleeps" or pauses some or all operations. During a typical sleep function the CPU clock of the microcontroller stops operating to conserve battery power*" (page 3, last paragraph). The specification also recites, "*In the current embodiment the sleep function is a*

standard function performed by microcontroller 232 in which execution of instructions are halted. The sleep function is commonly used to conserve power" (page 30, paragraph 3). The teachings in Nemecek as well as the teachings of a sleep function in Applicant's specification disclose that the sleep function is commonly known in the art. Because the sleep function is "*performed by the microcontroller*", one of ordinary skill in the art would reasonably conclude that the performance of a sleep function would be performed by receiving some "signal" from an operating program running on the microcontroller that would indicate a necessity to perform a sleep function at some point in time as determined by the operating program running on the microcontroller ("how" and "when"). Since it is taught that "*during a typical sleep function the CPU clock of the microcontroller stops operating..*", one of ordinary skill in the art would reasonably conclude that one or more clocks of the device under test would be turned off by the sleep function, and that the microcontroller in the sleep state would discontinue execution of instructions that are performed in lockstep with an emulator device since in the sleep state, the microcontroller "*pauses some or all operations*". Therefore, the Examiner concludes that the limitations set forth in Claim 1 as to "performing sleep operation" are inherent steps to performing a "sleep" operation or function as disclosed in Applicants specification and set forth in Nemecek.

21. Applicant argues that "Resetting the microcontroller, as taught by Nemecek, differs from initiating a sleep function..." (page 14, paragraph 2). The Examiner agrees with Applicant's argument, however, the Examiner discusses above how "turning off the

clocks" in response to the initiation of a sleep function disclosed as well known in the art.

22. Applicant argues that "...turning off the clocks in the microcontroller in response to detecting a watchdog timer expiration, as taught by Nemecek, fails to either teach or suggest "in response to the initiating the sleep function, turning off one or more clocks of the device under test" as claimed" (page 15, paragraph 1). The Examiner agrees with Applicant's argument, however, the Examiner discusses above how "turning off the clocks" in response to the initiation of a sleep function disclosed as well known in the art.

23. Applicant argues that "...Nemecek fails to teach or suggest that the first signal is generated by the device under test..." since "...the gatekeeper that is within the base station and is separate from the SUT sends a message informing the host computer of the sleep mode of the microcontroller..." (page 15, paragraph 3). The Examiner concludes that the limitation of claim 3, that is, "...wherein said first signal is generated by said device under test and is transmitted internally to a register that indicates that a sleep function is to be performed", is inherent to the performance of a sleep function as discussed above.

24. Applicant's arguments, see page 16, paragraphs 2 and 3, filed 12/11/07, with respect to Claims 4, 13 and 26 have been fully considered and are persuasive. The rejection of Claims 4-6, 13-15, 26-28 under 35 U.S.C. 102(e) as being anticipated by Nemecek et al have been withdrawn.

25. Applicant's arguments, see pages 17-16, filed 12/11/07, with respect to Claims 7, 16 and 21 have been fully considered and are persuasive. The rejection of Claims 7-9, 16-24 under 35 U.S.C. 102(e) as being anticipated by Nemecek et al have been withdrawn.

26. Applicant's arguments, see pages 18-19, filed 12/11/07, with respect to Claims 9, 19 and 22 have been fully considered and are persuasive. The rejection of Claims 9, 19 and 22 have been withdrawn.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on Tuesday-Thursday, 7AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Mary C. Jacob
Examiner
AU2123

MCJ
1/22/08

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